Amendments of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (CURRENTLY AMENDED) A method of operating a data processing device (100)~~, notably a chip card,~~ which includes an integrated circuit (10) which executes useful arithmetic ~~operations, notably~~ cryptographic operations, in dependence on a first clock signal, characterized in that:

a second clock signal is derived from the first clock signal under random control so as to be applied to the integrated circuit (10) instead of the first clock signal while distances between clock edges of the second clock signal vary at random in time; and

the integrated circuit (10) is randomly switched between different modes of operation, the different modes of operation including at least two calculation methods which produce an identical result while using different arithmetical approaches.

2. (CANCELED)

3. (CANCELED)

4. (CURRENTLY AMENDED) A method as claimed in Claim ~~3~~1, characterized in that the ~~various~~ different modes of operation further include at least one dummy mode of operation ~~"dummy"~~ (32) in which the integrated circuit (10) does not execute useful operations but dummy arithmetic operations which act on predetermined or random input data, the result being rejected and not taken up in the results or input data for the useful arithmetic operations.

5. (CURRENTLY AMENDED) A method as claimed in Claim 4, characterized in that the ~~various~~ different modes of operation further include a deactivated mode ~~"deactivated"~~ (36) in which the integrated circuit (10) does not execute arithmetic operations.

6. (CURRENTLY AMENDED) A data processing device (100)~~, notably a chip card,~~ which ~~is specifically intended to carry out a method as claimed in at least one of the preceding Claims and~~ includes an integrated circuit (10) which executes useful arithmetic ~~operations, notably~~ cryptographic operations, in dependence on the first clock signal (18), characterized in that:

the device is provided with a clock control unit (14) which is connected to the integrated circuit (10) as well as with a random generator (12) which is connected to the clock control unit (14), the clock control unit (14) being constructed in such a manner that it generates a second clock signal (20) in dependence on the random generator (12) and the first clock signal (18), which second clock signal varies at random and controls the integrated circuit (10); and

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the clock control unit (14) is further constructed in such a manner that it switches, in dependence on the random generator (12), the integrated circuit (10) between different modes of operation (30, 32, 34, 36) on a random basis, the different modes of operation (30, 32, 34, 36) including at least two calculation methods (30, 34) which produce an identical result while using different arithmetical approaches.

7. (CANCELED)

8. (CANCELED)

9. (CURRENTLY AMENDED) A data processing device (100) as claimed in Claim ~~8~~6, characterized in that, the ~~various~~ different modes of operation (30, 32, 34, 36) further include at least one dummy mode of operation ~~"dummy"~~ (32) in which the integrated circuit (10) does not execute useful operations but dummy arithmetic operations which act on predetermined or random input data, the result not being taken up in results or input data for the useful arithmetic operations.

10. (CURRENTLY AMENDED) A data processing device (100) as claimed in Claim 9, characterized in that the ~~various~~ different modes of operation (30, 32, 34, 36) include a deactivated mode ~~"deactivated"~~ (36) in which the integrated circuit (10) does not execute arithmetic operations.

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11. (CURRENTLY AMENDED) A data processing device (100) as claimed in Claim 10, characterized in that in at least one further mode of operation, ~~the~~a time base (16) is additionally distorted so that the summing according to the "Differential Power Analysis" method is additionally impeded or made impossible.